Power System Redesign

# Abstract

Revisions of the adequacy of the current power distribution topology (Product point B1.2) has revealed potential flaws in both function and failure immunity. A new concept has been put forward that is believed to be simpler, more robust and would add redundancy required on the satellite. A new task of duration 2 weeks has been allocated to a feasibility investigation and initial prototype testing.

# Scope

This document justifies the addition of task 2.4.12 Power System Redesign onto the BLUEsat Project Gantt Chart. The following will detail the inadequacies identified in the current design due to further testing and analysis and briefly outline the proposed system and its benefits.

This document will also outline a brief project plan for this task from research to prototype construction.

This document does not contain technical detail of either the current or proposed designs. These will be submitted in future as design documents and drawings integrated into the BLUEsat SVN.

# Current Design

The current overall power distribution topology was optimised for the original intended 18 month flight plan. The system placed an emphasis on high-frequency on/off switching to cycle through components and to extend battery life.

Analysis of the required performance of the satellite on the balloon has revealed that for the stated maximum flight time of 7 days, this switching is no longer necessary.

Furthermore, the current design only allows for limited power regulation to the RF transmitters on the satellite due to unforeseen frequency drift. A greater degree of control would require a different regulation mechanism.

# Proposed Design

The proposed design moves away from the use of Switching Regulators and Low-Dropout Regulators and toward the use of Ideal Diode Power/Or Controller in conjunction with Switching Regulators. See Figure 1 a) and b) for a basic illustration of the old and new design.

The proposed design will add redundancy, use less components and can be achieved using more well known designs. Notably, all LDOs have been excluded as the function of switching discrete subsystems off has become superfluous.

More technical documentation will be submitted in future detailing the full system design.

# Project Plan

Extra time and resources have been allocated to address this project such that it does not affect the other tasks on hand.

Team members are currently donating extra time in order to meet the extra goals brought on by this project.

## Week 1 – Saturday 09/06/2012 – Friday 15/06/2012

* Overall design
* Chip Selection
* Schematic creation
* Board Design
* Review

## Week 2 – Saturday 16/06/2012 – Friday 22/06/2012

* Prototype Creation
* Testing
* Design Review

## Project End – Saturday 23/06/2012

* Major Review
* Integration into the rest of the Satellite.